Remarks

In the Office Action, the Examiner noted that claims 1-63 are pending in the application, and that claims 1-63 are rejected. By this amendment, claims 9, 16, 46, 54, 57, and 60 have been amended. Thus, claims 1-63 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

The Title has been amended as required by the Examiner.

In the specification, the table on page 1 has been amended to identify the co-pending applications by their serial numbers.

In the Claims

Rejection Under 35 USC 112 second paragraph

The Examiner rejected claim 9 under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicant has amended the claim to distinctly claim the subject matter that Applicant regards as his invention.

Rejection Under 35 USC 102(b)

The Examiner rejected claims 16, 18-33, and 36-45 under 35 U.S.C. § 102(b), as being anticipated by *Stiles, et al.*, U.S. Patent No. 5,163,140 (hereinafter *Stiles*). Applicant respectfully traverses the rejection of claims 16, 18-33, and 36-45.

With respect to claim 16, the Examiner asserted that *Stiles* teaches a speculative BTAC, coupled to an address bus, that provides a speculative target address of a previously executed branch instruction in response to a fetch address on the address bus that selects a line of instruction bytes from an instruction cache whether or not the previously executed branch instruction is present in the line of instruction bytes. Applicant respectfully asserts that *Stiles* does not teach a speculative BTAC, coupled to an address bus, that provides a speculative target address of a previously executed branch instruction in response to a fetch address on the address bus that selects a line of instruction bytes from an instruction cache in parallel with the instruction cache providing the line of

instruction bytes, and control logic that controls a multiplexer to select the speculative target address as the fetch address during a first period whether or not the previously executed branch instruction is present in the line of instruction bytes, as recited by amended claim 1 for the following reasons.

1. First, *Stiles* specifically teaches that the address of the branch instruction being decoded (32-bit decode PC of Fig. 2) is used to perform the lookup in his branch prediction cache (BPC) to communicate a target address. Col. 9, lines 38-66. In contrast, the instruction cache is accessed using a fetch address via a 52-bit physical address bus. Col. 10, lines 3-5; Figs. 1 and 2, element 55. Hence, Applicant can find no teaching in *Stiles* of the BPC providing a target address in response to an instruction cache fetch address provided on an address bus in parallel with an instruction cache providing a cache line of instruction bytes in response to the fetch address.

2. Second, *Stiles* specifically teaches that the decode PC used to perform the BPC lookup is a delayed version of the fetch address (col. 9, lines 41-44); hence, the BPC cannot be providing a speculative target address in parallel with the instruction cache providing the line of instruction bytes for which the speculative target address is being provided.

3. Third, Applicant can find no teaching in *Stiles* of control logic that controls a multiplexer to select the speculative target address of the branch instruction as the fetch address whether or not a branch instruction is present. *Stiles* does teach that a predicted address is not guaranteed to be correct and must eventually be checked elsewhere in the pipeline. Col. 16, lines 31-35. In addition, *Stiles* teaches that the decode PC looked up in the BPC may be for non-branch instructions since the decoding of the instruction at the decode PC is performed in parallel with the BPC lookup. Col. 9, lines 58-62. However, this is different from, and Applicant can find no teaching in *Stiles* of, a predicted target address being incorrect because it is not known whether there is a branch instruction present in the instruction cache line selected by the fetch address, much less control logic that selects a speculative target address of a branch instruction as a next instruction cache fetch address whether or not the branch instruction is present in a cache line selected by the previous fetch address. Indeed, Applicant respectfully asserts that *Stiles* teaches away from selecting a predicted target address as a fetch address without knowing whether a

branch instruction is present in the cache line by implicitly teaching that branching is performed after decoding to determine that a branch instruction is present for the following reasons.

First, *Stiles* teaches that the BPC is accessed in parallel with the decode of the instruction whose address (decode PC) is being used to make the target address prediction (col. 5, lines 11-12; col. 9, lines 58-60; col. 11, lines 30-34), which implies that by the time the predicted target address is available, the result of the instruction decode, i.e., whether the instruction is a branch instruction or not, would also be available for deciding whether to use the predicted target address as the next fetch address or to continue fetching the next sequential cache line, i.e., whether to branch or not branch.

Second, *Stiles* teaches, "[t]here is no substantive difference between whether the prediction was based on cached information from an earlier execution of this branch or from some other branch" (col. 17, lines 22-25), implying that the BPC knows at least that a branch instruction was present in the current instruction stream at the decode PC.

Third, branching based on *Stiles*' second level BPC would result in very poor branch prediction performance unless it was known that the instruction for which the target address was being predicted is a branch instruction. *Stiles*' BPC is a two-level BPC. The first level BPC indicates a hit if the instruction decode PC matches a tag stored in each entry of the first level BPC. Col. 3, line 62 to col. 4, line 2; col. 14, lines 3-13. If the instruction decode PC misses in the first level BPC, then the predicted target address provided by the second level BPC is used. Col. 17, lines 3-6. However, the second level BPC contains no tags; rather, the second level BPC assumes a tag match of the instruction decode PC and always is a hit. Col. 4, lines 30-37; col. 16, lines 22-30; col. 17, lines 6-8. That is, every decode PC hits in the second level BPC, including non-branch instructions; thus the processor would branch for every single instruction whose decode PC selects an entry in the second level BPC whose direction bit indicates a taken branch, which would result in many mispredictions – unless, of course, the processor only branches if it decodes the instruction first and determines that a branch instruction is present at the decode PC and does not branch if a non-branch instruction is present, as Applicant asserts *Stiles* implicitly teaches.

4. Finally, Applicant can find no teaching in *Stiles* of the address select circuitry cited by the Examiner in Fig. 8 to perform the function of selecting a speculative target address as a fetch address for selecting a line of instruction bytes in an instruction cache as recited in claim 16. Rather, *Stiles*' teaches the address select circuitry of Fig. 8 selects multiple different lines in the first level BPC for performing multiple simultaneous reads and/or writes on the different selected lines in the same cycle since, for example, in the same cycle the BPC may need to be read in order to make a prediction and also may need to be updated in response to completion of a branch instruction. Col. 13, line 58 to col. 14, line 2. Eight possible operations to read or write the BPC may be performed as described in detail at col. 14, line 3 to col. 15, line 23. However, none of these operations is selecting a speculative target address as a fetch address for selecting a line of instruction bytes in an instruction cache as recited in claim 16.

For the reasons stated above, Applicant respectfully asserts that *Stiles* does not anticipate claim 16.

Applicant respectfully asserts *Stiles* does not anticipate dependent claims 17-45 because they depend from independent claim 16, which is not anticipated by *Stiles* for the reasons discussed above.

Rejection Under 35 USC 103

Claims 1-6, 10-15, 17, 46-53, and 57-63

The Examiner rejected claims 1-6, 10-15, 17, 46-53, and 57-63 under 35 U.S.C. § 103, as being unpatentable over *Stiles* in view of *Gochman, et al.*, U.S. Patent No. 5,964,868 (hereinafter *Gochman*). Applicant respectfully traverses the rejection of claims 1-6, 10-15, 17, 46-53, and 57-63.

With respect to claim 1, the Examiner asserts that *Stiles* has taught a storage element for storing an indication of whether the microprocessor branched to the speculative target address provided by the BTAC without knowing whether an instruction associated with the indication is a branch instruction, and prediction check logic for notifying branch control logic that the microprocessor erroneously branched to a speculative target address if instruction decode logic indicates the instruction is not a branch instruction and the

indication indicates the microprocessor branched to the speculative target address. Applicant respectfully asserts that *Stiles* has not taught a storage element for storing an indication of whether the microprocessor branched to the speculative target address provided by the BTAC without knowing whether an instruction associated with the indication is a branch instruction, nor prediction check logic for notifying branch control logic that the microprocessor erroneously branched to a speculative target address if instruction decode logic indicates the instruction is not a branch instruction and the indication indicates the microprocessor branched to the speculative target address.

As discussed above with respect to claim 16, Applicant can find no teaching in *Stiles* of the microprocessor branching to a predicted target address provided by the BPC of *Stiles* until decoding the instruction and therefore knowing that the instruction pointed to by the decode PC used to make the target address prediction is a branch instruction. The Examiner cites portions of *Stiles* that state a tag is associated with each pseudo-op (decoded instruction word) that uniquely identifies the pseudo-op and is used in exception handling generally. Col. 5, lines 15-33; col. 6, line 59 to col. 7, line 30. However, *Stiles* does not teach the tag indicating whether the microprocessor branched to a predicted target address provided by the BPC without knowing whether an instruction associated with the indication is a branch instruction, much less handling an exception condition associated with such a condition. This is not surprising since, as discussed above with respect to claim 16, Applicant asserts that *Stiles* implicitly teaches that his processor does not branch based on the BPC-predicted target address unless it knows from decoding the instruction that the instruction at the decode PC is a branch instruction. Although the Examiner cites text in *Stiles* that a predicted address is not guaranteed to be correct and must eventually be checked elsewhere within the CPU, this text does not teach branching to the BPC-predicted target address without knowing whether the instruction was a branch instruction, but only teaches that the predicted address may be incorrect, for example because it is the target address of some other branch instruction whose lower address bits map to the same entry in the direct-mapped, tagless second level BPC. Col. 17, lines 22-25.

Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate dependent claims 2-13 because they depend from independent claim 1, which is not anticipated or obviated by *Stiles* in view of *Gochman* for the reasons discussed above.

Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate independent claim 14 for the same reasons discussed above with respect to claim 1. Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate dependent claim 15 because it depends from independent claim 14, which is not anticipated or obviated by *Stiles* in view of *Gochman* for the reasons discussed above.

Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate dependent claim 17 because it depends from independent claim 16, which is not anticipated or obviated by *Stiles* in view of *Gochman* for the reasons discussed above.

Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate claim 46 as amended for the reasons discussed above with respect to claims 1, 14, and 16. Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate dependent claims 47-49 because they depend from independent claim 46, which is not anticipated or obviated by *Stiles* in view of *Gochman* for the reasons discussed above.

Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate claim 50 for the reasons discussed above with respect to claims 1, 14, and 16. Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate dependent claims 51-53 because they depend from independent claim 50, which is not anticipated or obviated by *Stiles* in view of *Gochman* for the reasons discussed above.

Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate claim 57 as amended for the reasons discussed above with respect to claims 1, 14, and 16. Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate dependent claim 58 because it depends from independent claim 57, which is not anticipated or obviated by *Stiles* in view of *Gochman* for the reasons discussed above.

Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate claim 59 for the reasons discussed above with respect to claims 1, 14, and 16.

Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate claim 60 as amended for the reasons discussed above with respect to claims 1, 14, and 16.

Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate claims 61-63 for the reasons discussed above with respect to claims 1, 14, and 16.

Claims 34 and 35

The Examiner rejected claims 34 and 35 under 35 U.S.C. § 103, as being unpatentable over *Stiles* in view of *Gochman* and *Fite et al.*, U.S. Patent No. 5,142,634 (hereinafter *Fite*). Applicant respectfully traverses the rejection of claims 34 and 35. Applicant respectfully asserts *Stiles* in view of *Gochman* and *Fite* does not anticipate or obviate dependent claims 34 and 35 because they depend from independent claim 16, which is not anticipated or obviated by *Stiles* in view of *Gochman* and *Fite* for the reasons discussed above.

Claims 7 and 54-56

The Examiner rejected claims 7 and 54-56 under 35 U.S.C. § 103, as being unpatentable over *Stiles* in view of *Gochman* and *Fite*. Applicant respectfully traverses the rejection of claims 7 and 54-56.

Applicant respectfully asserts *Stiles* in view of *Gochman* and *Fite* does not anticipate or obviate dependent claim 7 because it depends from independent claim 1, which is not anticipated or obviated by *Stiles* in view of *Gochman* for the reasons discussed above.

Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate claim 54 as amended for the reasons discussed above with respect to claims 1, 14, and 16. Applicant respectfully asserts *Stiles* in view of *Gochman* does not anticipate or obviate dependent claims 55-56 because they depend from independent claim 54, which is not anticipated or obviated by *Stiles* in view of *Gochman* for the reasons discussed above.

Claims 8 and 9

The Examiner rejected claims 8 and 9 under 35 U.S.C. § 103, as being unpatentable over *Stiles* in view of *Gochman* and *Brown et al.*, U.S. Patent No. 5,964,868 (hereinafter *Brown*). Applicant respectfully traverses the rejection of claims 8 and 9. Applicant respectfully asserts *Stiles* in view of *Gochman* and *Brown* does not anticipate or obviate

claims 8 and 9 because they depend from independent claim 1, which is not anticipated or obviated by *Stiles* in view of *Gochman* for the reasons discussed above.

The Examiner has indicated additional prior art which is made of record and not relied upon. None of these references anticipate or obviate applicant's invention.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Applicant earnestly requests the examiner to telephone him at the direct dial number printed below if the examiner has any questions or suggestions concerning the application.

Respectfully submitted,

James W. Huffman
Huffman Law Group, P.C.
Registration No. 35,549
Customer No. 23669
1832 N. Cascade Ave.
Colorado Springs, CO 80907
719.475.7103
719.623.0141 fax
jim@huffmanlaw.net

Date: 9-20-04

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By: Vicki J. Hoge